REMARKS

AMENDMENT TO SPECIFICATION

The specification has been amended pursuant to 37 CFR §1.117) to secure correspondence between the claims and the specification. In particular, claim 26 as originally filed with parent application 09/191,215, stated that "the die attach area has an outline corresponding to an outline of the die". Accordingly this phrase has been incorporated at page 11, line 23-25 of the specification as follows:

"The solder mask 80B includes a die attach opening 86 having an outline corresponding to but only slightly larger than the outline of the semiconductor die 16

In addition, the recitation "substantially matching" in the independent claims has been changed to "corresponding to but only slightly larger than". Although, the terms "matching" and "corresponding" are synonymous, the claims have been amended to secure correspondence with the original disclosure. (See definition for correspond in "Webster's College Dictionary" and "Roget's II The New Thesaurus" which are provided with the IDS being filed with the present Amendment.)

Claim Rejections Under 35 USC §103

Claims 24-36 have been rejected under 35 USC 103(a) as being unpatentable over the admitted prior art (APA) in view of Lee et al. (U.S. Patent No. 5,796,586) and/or Akram et al. (US Patent No. 5,739,585).

In response to the 35 USC §103 rejections, the claims have been amended. In addition, the Examiner is asked to consider the arguments to follow.

Summary of the Invention

The claims are directed to a board-on-chip semiconductor package 62 (Figure 6B). As shown in Figure 6B, the BOC

package 62 includes a substrate 56 comprising a first surface 44 with a pattern of conductors 48, an opposing second surface 46 with a die attach area 50, and a wire bonding opening 64 extending through the substrate 56 from the first surface 44 to the second surface 46. In addition, the package 62 includes a first solder mask 80A having openings 82 for attaching solder balls 88 to the conductors 48, and an opening 84 (Figure 3C) for wire bonding to the conductors 48. The package 62 also includes a second solder mask 80B having an opening 86 (Figure 3D) on the die attach area 50.

As also shown in Figure 6B, the package 62 includes a semiconductor die 16 placed face down (circuit side down) through the opening 86 in the second solder mask 80B, and attached directly to the substrate 56 in the die attach area 50. An adhesive layer 72 (Figure 6A) attaches the face of the die 16 directly to the substrate 56. The package 62 also includes wires 94 placed through the wire bonding opening 64 in the substrate 56, and bonded to bonding pads on the face of the die 16, and to bonding pads 52 (Figure 6A) on the conductors 48. In addition, solder balls 88 are placed through the openings 82 in the first solder mask 80A, and attached to ball bonding pads 54 (Figure 6A) on the conductors 48. As also shown in Figure 6B, an encapsulating resin 90 is molded over the die 16, and over the second solder mask 80B. Further, a glob top 92 can be placed over the wires 94, and in the wire bonding opening 64 to protect the wire bonds.

Argument

35 USC §103 Rejections Over Admitted Prior Art and Lee et al.

The admitted prior art discloses a board-on-chip package 10 (Figure 1A) in which the die 16 is bonded face down to the solder mask 22, rather than directly to the substrate in an open die attach area as presently claimed.

Lee et al. discloses a substrate board 200 (Figure 7) having conductive traces 202, and a solder mask 218' which is configured to protect the conductive traces (column 7, lines 56-58). However, the solder mask 218' in Lee et al. must leave the tips of the conductive traces exposed for wire bonding (column 8, lines 6-7). In addition, the die must be spaced from these tips in order to provide room for the wires that are wire bonded to the die and to the tips. These wires are several milli meters long, and the exposed tips of the conductive traces add to this length. Accordingly, the die attach area 204 in Lee et al. would need to be significantly larger than the outline of the die. Similarly, in the embodiments illustrated in Figures 3, 4 and 5 of Lee et al., the solder mask 218 only covers the edges of the substrate board 200.

With the presently claimed package, the opening 86 (Figure 7) in the second mask 80B (Figure 7) has "an outline corresponding to but only slightly larger than the outline of the die". In addition, the amended independent claims state that the encapsulating resin 90 (Figure 7) is "on the die" and "on the second mask". This construction provides an improved package because the encapsulating resin 90 adheres mainly to the second mask, because there is very little space between the die and the solder mask.

In Lee et al. the encapsulating material 224 (Figure 6) is deposited on a relatively large area of the substrate, which may not provide the same adhesion as the solder mask. With the present arrangement the solder mask 80B can comprise a high adhesion resist (e.g., Taiyo PSR-4000 resist described at page 10 lines 15-18 of the present specification), and a larger surface area for adhesion to the resist is provided.

Applicant would further argue that one skilled in the art at the time of the invention would have no incentive to combine the admitted prior art package, and Lee et al. in the manner of the Office Action. The Examiner has cited the teaching at column 7, line 60, of Lee et al. of the solder

mask providing better resistance to cracking, as the proposed motivation. However, the discussion at column 7, lines 56-63 of Lee et al. is a comparison of polyimide solder masks and high adhesion solder masks. This passage states that low cost polyimide solder masks "are more resistive to cracking at a location under substrate board 22 than their expensive "highly adhesive" counterparts". Accordingly, Applicant cannot understand how one skilled in the art reading this passage of Lee et al. would be motivated to open the solder mask in the admitted prior art package to define a die attach area.

35 USC §103 Rejections Over Admitted Prior Art and Akram et al. '585

Akram et al. '585 was cited as teaching "using conventional die attach technique where the die (18 in Fig. 10; Col. 9, line 24) is face bonded to the second surface using typical adhesive/fill materials (Col. 4, line 26) such as an epoxy, silicone, polyimide, other dielectric material, etc."

Admittedly face bonding of a die to a substrate is known in the art. However, the presently claimed package also includes a solder mask having an opening which defines the die attach area. As Akram et al. '585 does not teach or suggest a solder mask with an opening defining a die attach area, the combination of the admitted art and Lee et al. would not have the same features as presently claimed. Also, as previously argued, the presently claimed solder mask provides improved adhesion for the encapsulating material because the solder mask provides a relatively large, highly-adhesive surface.

In addition, although die attach adhesives including filled adhesives are known in the art, the presently claimed filled adhesive in combination with a solder mask having an opening which defines a die attach area, is submitted to be unobvious over the art. Applicant would further argue that since Akram et al. '585 does not teach any solder masks,

there would be no motivation for one skilled in the art to combine Akram et al. '585 with the admitted prior art package.

Conclusion

In view of the above arguments and amendments, favorable consideration and allowance of claims 24-36 is respectfully requested. An Information Disclosure Statement is also being filed with this Amendment. Should any issues arise that will advance this case to allowance, the Examiner is asked to contact the undersigned by telephone.

Dated this 23rd day of July, 2001.

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CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class mail in an envelope addressed to: Assistant Commissioner of Patents, BOX AMENDMENT (FEE), Washington, D.C. on this 23rd day of July, 2001.

July 23, 2001
Date of Signature

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MARKED VERSION OF SPECIFICATION SHOWING CHANGES

On page 11, line 24, delete "that is" and substitute -- corresponding to but only--.

MARKED VERSION OF AMENDED CLAIMS SHOWING CHANGES

24. (four times amended) A semiconductor package comprising:

a substrate comprising a first surface, a second surface, a plurality of conductors and ball bonding pads on the first surface, and a bonding opening from the first surface to the second surface;

a semiconductor die having a first outline and a face on the bonding opening bonded directly to the second surface;

a first mask on the first surface comprising a plurality of via openings aligned with the ball bonding pads;

a second mask covering the second surface except in a die attach area defined by an opening through the second mask having a second outline [substantially matching] corresponding to but only slightly larger than the first outline;

an adhesive layer between the die and the substrate in the die attach area bonding the face to the second surface; [and]

a plurality of wires placed through the bonding opening and wire bonded to the die and to the conductors; and

an encapsulating resin on the die and on the second mask.

25. (four times amended) The package of claim 24 wherein the encapsulating resin comprises epoxy.
[further comprising an encapsulating material at least partially encapsulating the die and the second mask.]

27. (four times amended) A semiconductor package comprising:

a substrate comprising a first surface, a second surface, a plurality of conductors on the first surface comprising ball bonding pads and wire bonding pads, and a bonding opening from the first surface to the second surface;

a semiconductor die having a first outline, the die comprising a face on the bonding opening bonded to the second surface;

a first mask on the first surface comprising a plurality of via openings aligned with the ball bonding pads and a first opening exposing the wire bonding pads;

a second mask substantially covering the second surface comprising a second opening having a second outline [substantially matching] corresponding to but only slightly larger than the first outline to define an open die attach area on the second surface;

an adhesive layer between the die and the substrate in the open die attach area bonding the face to the second surface; [and]

a plurality of wires in the bonding opening wire bonded to the die and to the wire bonding pads; and

an encapsulating resin on the die and on the second mask.

30. (four times amended) A semiconductor package comprising:

a substrate having a first surface, a second surface and a bonding opening there through;

a plurality of conductors on the first surface comprising a plurality of ball bonding pads;

a first mask on the first surface comprising a plurality of via openings to the ball bonding pads;

a semiconductor die having a face on the bonding opening attached directly to the second surface;

a second mask covering the second surface except in a die attach area defined by an opening through the second mask having an outline [substantially matching] corresponding to but only slightly larger than that of the face;

a plurality of solder balls in the via openings bonded to the ball bonding pads; [and]

a plurality of wires placed through the bonding opening and bonded to the die and to the conductors; and

an encapsulating resin on the second mask encapsulating the die.

31. (four times amended) The package of claim 30 [further comprising an] wherein the encapsulating resin comprises epoxy.
[on the second surface at least partially encapsulating the die.]

34. (four times amended) A semiconductor package comprising:

a substrate comprising a first surface, an opposing second surface and a wire bonding opening from the first surface to the second surface;

a plurality of conductors on the first surface comprising wire bonding pads and ball bonding pads;

a first mask on the first surface comprising a plurality of via openings aligned with the ball bonding pads and a first opening exposing the wire bonding pads;

a semiconductor die aligned with the wire bonding opening and bonded face down to the second surface, the die having a first outline;

a second mask substantially covering the second surface and including an opening there through having a second outline [substantially matching] corresponding to but only slightly larger than the first outline to define an open die attach area on the second surface;

an adhesive layer between the die and the substrate in the open die attach area bonding the die directly to the second surface;

a plurality of wires placed through the wire bonding opening and bonded to the die and to the wire bonding pads; and

an encapsulating resin on the second mask [surface at least partially] encapsulating the die.